GR-LEON4-ITX
Development Board

User Manual

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REVISION HISTORY

Revision	Date	Page	Description
0.1 DRAFT	2010-03-01	All	New document
0.2	2010-03-17		Added reference to Quick Start Guide
0.3	2010-08-13		Added picture showing how to connect ribbon cable with DE-9 connector.

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1   INTRODUCTION

1.1 Overview

This document describes the *GR-LEON4-ITX* Development Board.

The purpose of this equipment is to provide developers with a convenient hardware platform for the evaluation and development of software for the *Aeroflex Gaisler LEON4* Processor.

The LEON4 processor is a synthesizable VHDL model of a 32-bit processor compliant to the SPARC V8 architecture. In this variant, Aeroflex Gaisler has implement a Dual Core LEON4 with a rich set of IP cores and interfaces in a eASIC structured ASIC running at 200 MHz on this board.

The *GR-LEON4-ITX* Development Board comprises a custom designed PCB in a Mini-ITX format, making the board suitable either for stand-alone bench top development, or if required, to be mounted in a 'standard' commercial Mini-ITX housing.

The principle interfaces and functions are accessible on the front and back edges of the the board, and secondary interfaces via headers on the board.
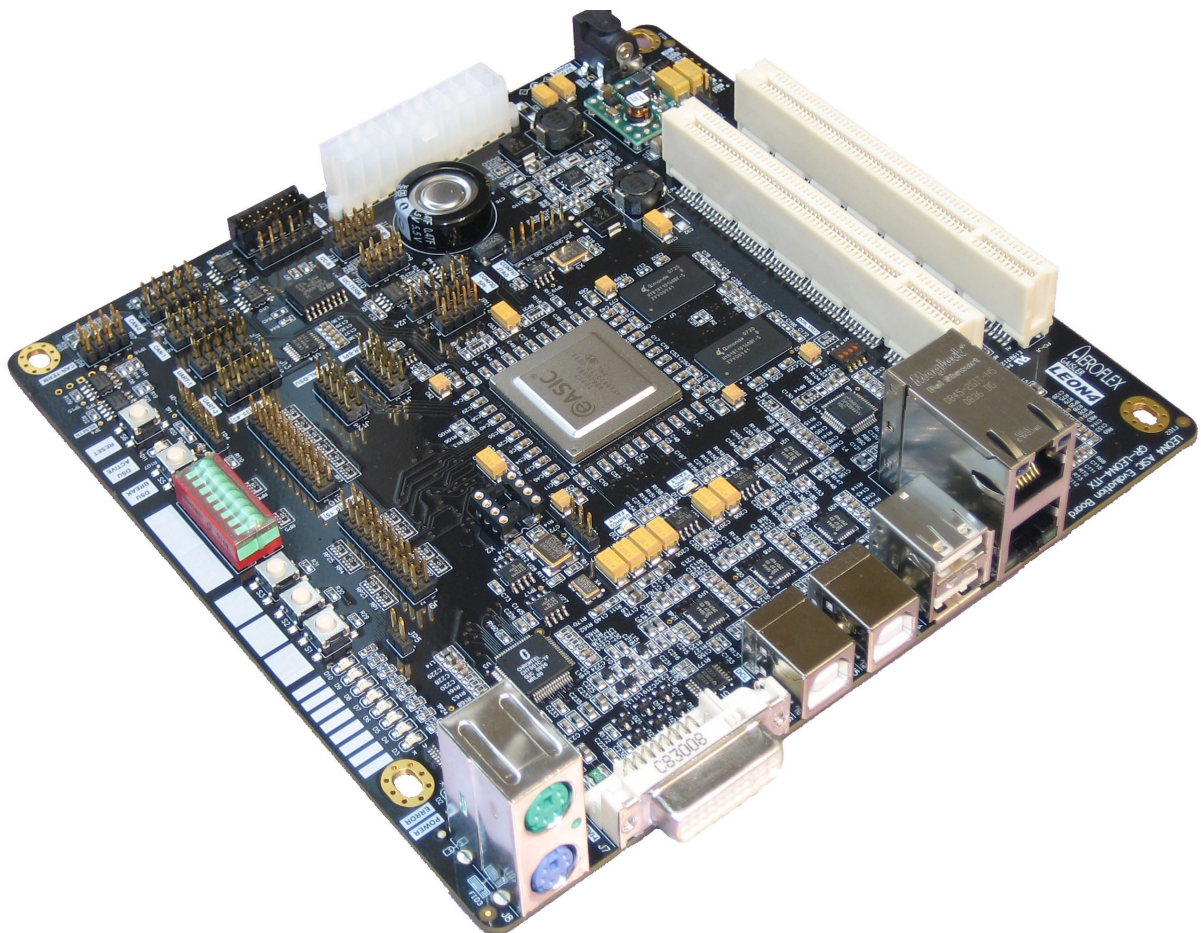
Figure 1-1: GR-LEON4-ITX Development Board

The PCB contains the following main items as detailed in section 2 of this document:

- LEON4 ASIC with Dual Core Leon4 architecture
- Memory
    - DDR2-400 RAM   256 MByte   (2x 1Gbit HYB18T1G160BF-5)
    - SPI program FLASH   64Mbit   (1x M25P64 SPI prom)
- Power, Reset, Clock and Auxiliary circuits
- Interface circuits required for the features listed below

The interface connectors on the Front edge of the board provide:

- Dual PCI (32 bit) mother-board slots
- Dual RJ45 10/100 Mbit RMII Ethernet interface (DP83848VV with RJ45 jack)
- Dual USB2.0 (USB-A) Host Interface (ISP1504A)
- USB2.0 Device (USB-B) Interface (ISP1504A)
- USB2.0 Debug Comm. Link (USB-B) Interface (ISP1504A)
- DVI-I (Analog and Digital) Video Interface (Chrontel CH7301C)
- PS2 Keyboard/Mouse Interface

The interface connectors on the Back edge of the board provide:

- +5V input power connector
- JTAG Debug interface

Additionally, on-board headers and components provide access to the following functions/ features:

- 44 pins General Purpose I/O pins
    - 25 on 0.1" pin headers
    - 8 on DIP switch
    - 3 on Push button switches
    - 8 connected to LED indicators
- I2C interface with on-board Real-Time Clock, and user connections on 0.1" header
- SPI interface, with on-board Temperature measurement, and user connections on 0.1" header
- Dual CAN bus interface (SN65HVD230)
- Two Serial UART interface (RS232) with D9 Sub female connectors
- ATX Style power connector

Debug interface support is demonstrated on the board with support for debugging via the following interfaces:

- Push Buttons for *RESET* and DSU-*BREAK*
- LED indicators for POWER, ERRORN, DSU Active
- Assorted jumpers and Test Points for configuration and Test of the board

To enable convenient connection to the interfaces, most connector types and pin-outs are compatible with the standard connector types for these types of interfaces.

Debug interface support is demonstrated on the board with support for debugging via the following interfaces:

- JTAG
- ETH (EDCL)
- USB (USB-DCL)
- SERIAL (LVTTL i/f)

1.2 References

RD-1   GR-LEON4-ITX_schematic.pdf, Schematic

RD-2   GR-LEON4-ITX_assy_drawing.pdf, Assembly Drawing

RD-3   GR-LEON4-ITX_bom.pdf, Bill of Materials

RD-4   LEON4-ASIC-DEMO Data Sheet and User's Manual

RD-5   GRMON User Manual

RD-6   GR-LEON4-ITX Quick Start Guide

1.3 Handling

ATTENTION : OBSERVE PRECAUTIONS FOR

HANDLING ELECTROSTATIC SENSITIVE DEVICES

This unit contains sensitive electronic components which can be damaged by Electrostatic Discharges (ESD). When handling or installing the unit observe appropriate precautions and ESD safe practices.

When not in use, store the unit in an electrostatic protective container or bag.

When configuring the jumpers on the board, or connecting/disconnecting cables, ensure that the unit is in an un-powered state.

1.4 Abbreviations

ASIC   Application Specific Integrated Circuit.
DIL   Dual In-Line
DDR   Double Data Rate
DSU   Debug Support Unit
ESD   Electro-Static Discharge
GPIO   General Purpose Input / Output
I/O   Input/Output
IP   Intellectual Property
MUX   Multiplexer
PCB   Printed Circuit Board
RMII   Reduced Media Independent Interface
SOC   System On a Chip

2 ELECTRICAL DESIGN

2.1 LEON4 ASIC

The Aeroflex Gaisler LEON4 processor core is a synthesizable VHDL model of a 32-bit processor compliant with the SPARC V8 architecture. The core is highly configurable and particularly suitable for high performance multi-core system-on-a-chip (SOC) designs.

The core is interfaced using the AMBA 2.0 AHB bus and supports the IP core plug&play method provided in the Aeroflex Gaisler IP library (GRLIB). The processor can be efficiently implemented on FPGA and ASIC technologies and uses standard synchronous memory cells for caches and register file. The processor supports the MUL, MAC and DIV instructions and an optional IEEE-754 floating-point unit (FPU) and Memory Management Unit (MMU). The LEON4 cache system consists of separate I/D multi-set Level-1 (L1) caches with up to 4 ways per cache, and an optional Level-2 (L2) cache for increased performance in data intensive applications. The LEON4 pipeline uses 64-bit internal load/store data paths, with an AMBA AHB interface of either 64- or 128-bit. Branch prediction, 1-cycle load latency and a 32x32 multiplier results in a performance of 1.7 DMIPS/MHz, or 2.1 Coremark/MHz.

The wider interfaces provides higher bus and memory bandwidth which is necessary when designing ASICs with high clock frequencies (800 MHz and above). The LEON4 is fully software compatible with previous LEON processors. The configurability of LEON4 allows designers to optimize the processor for performance, power consumption, I/O throughput, silicon area and cost.
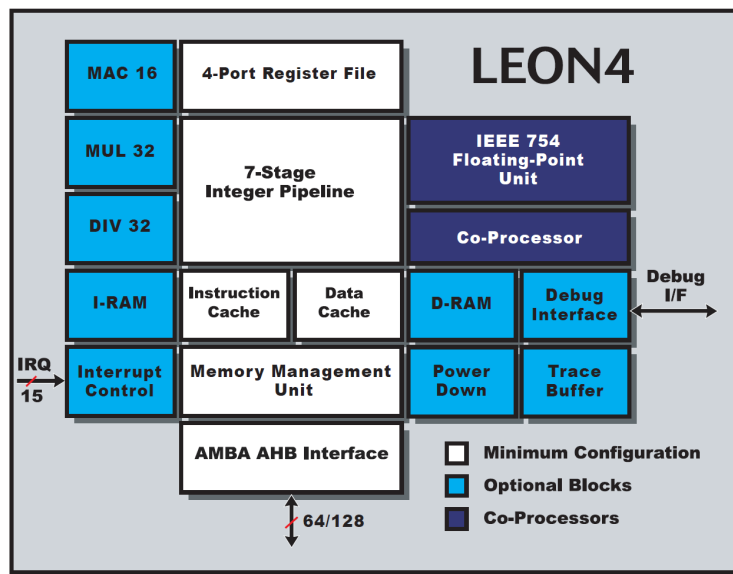
Figure 2-1: LEON4 Core Block Diagram

As a technology demonstrator, Aeroflex Gaisler has implemented a representative LEON4 configuration in a Structured ASIC from eASIC technologies.

This design consists of dual core LEON4 processors and a set of IP cores connected through AMBA AHB/APB buses as represented in Figure 2-2.
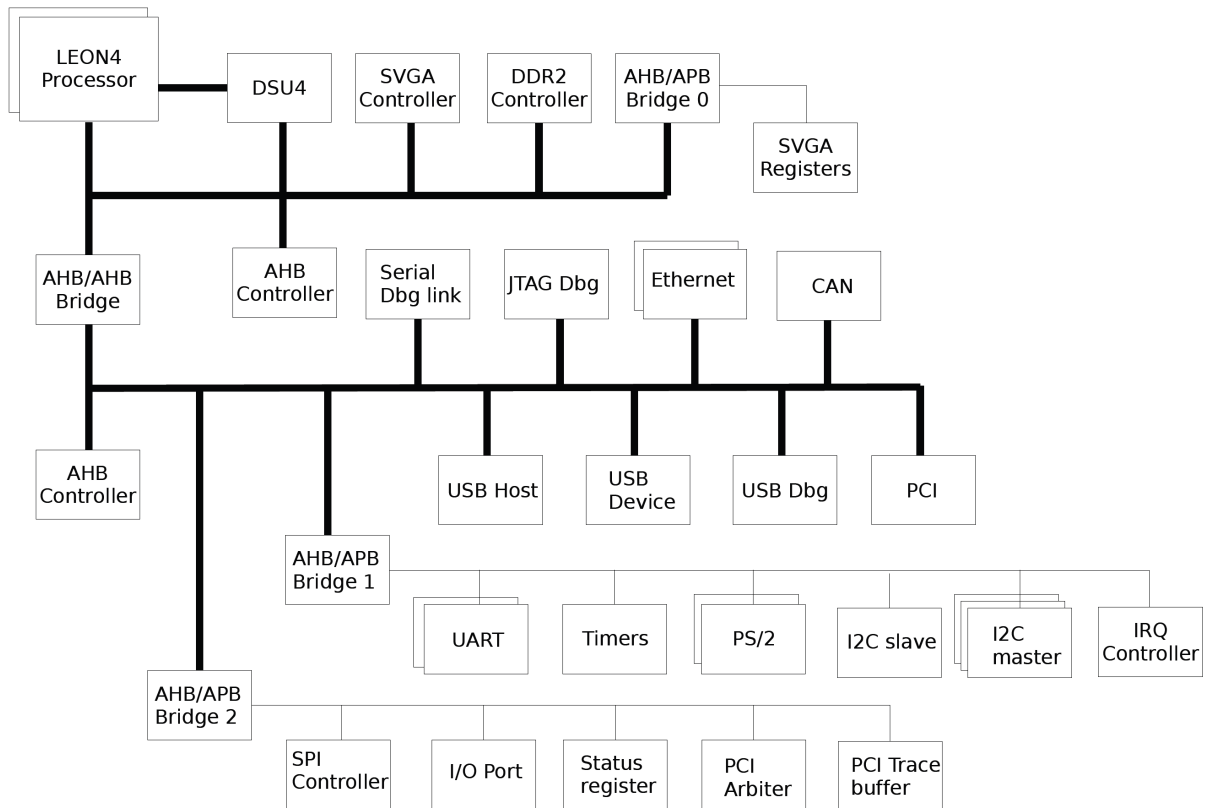
Figure 2-2: LEON4 SOC Block Diagram

This LEON4 ASIC is packaged in a 672-pin, 1mm pitch Flip Chip Ball Grid Array package , and is soldered on to the PCB.

Details of the interfaces, operation and programming of the LEON4 ASIC is given in the *LEON4-ASIC-DEMO Data sheet and User's Manual,* RD-4, and in RD-5.

Figure 2-3: LEON4-ASIC-DEMO

2.2 Board Block Diagram

The *GR-LEON4-ITX* Board provides the electrical functions and interfaces as represented in the block diagram, Figure 2-4.
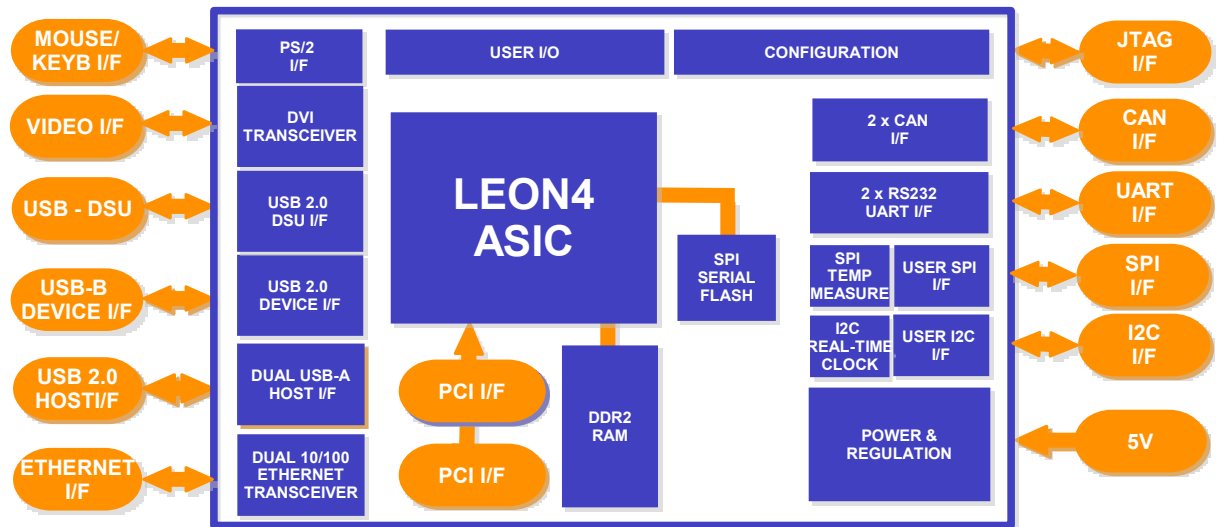
Figure 2-4: Block Diagram of GR-LEON4-ITX board

The Main PCB is a Mini-ITX format board (170 x 170mm) and can be used 'stand-alone' on the bench-top simply using an external +5V power supply.

2.3 Memory

The memory configuration installed on the board comprises:

- 2 Gbit (256Mbyte) of DDR2-400 RAM memory, organised as 1 bank x 64Mword x 32 bits wide
- 64Mbit of Flash PROM, in serial SPI flash device

DDR2 RAM

Two 16 bit wide DDR2 memory devices are included on the board (Hynix 1Gbit HYB18T1G160BF-5), providing 32 bit data connection to the processor with a total of 256MByte of volatile RAM memory.

SPI FLASH

A single Serial Flash PROM device (Intel/Numonyx M25P64-VMF6TP) is installed on the board, connected to the *SPIM* SPI interface of the processor.

This device provides 64Mbit of Non-Volatile storage, organised as 8Mbyte x 8 bits.

This device can be used for Program storage or as a boot device for the board.

2.4 PCI Slots

The *LEON4* ASIC device incorporate*s a GRPCI* Fast 32-bit PCI bridge core which functions as the PCI Host Controller on the *LEON4-ITX* Board.

To allow this board to function as a PCI motherboard, this board includes two 32 bits, 33MHz PCI motherboard slot connectors, PCI-J1 and PCI-J2.

Note that the PCI slots are intended for cards which are compatible with 3.3V PCI signalling voltage levels.

2.5 Ethernet Interface

The *LEON4* ASIC device incorporates two Ethernet controllers with support for RMII interface, and the *GR-LEON4-ITX* Development Board has two National Semiconductor DP83848 10/100Mbit/s Ethernet PHY transceivers. These are connected to a dual RJ45 connector are on board.

For more information on the registers and functionality of the Ethernet MAC+PHY device please refer to the data sheet for the *DP83848* device.

The RMII Ethernet PHY's are provided with a 50 MHz clock derived from the oscillator X1 on the board.
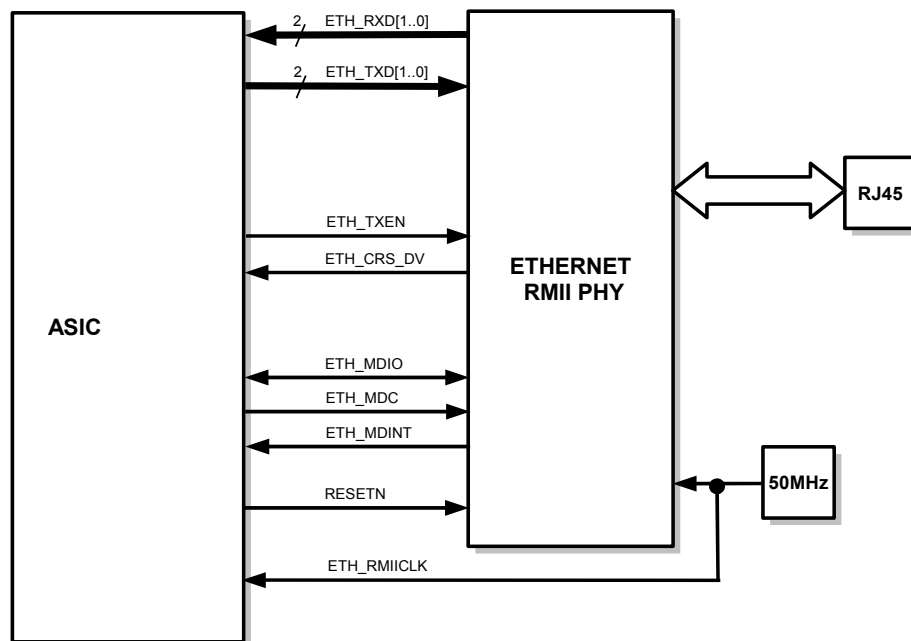
Figure 2-5: Block diagram of Ethernet RMII Interface

(one of 2 interfaces shown)

2.6 USB Host

The *LEON4* ASIC device includes two USB 2.0 Host interfaces, and these are connected to two on-board ISP1504 USB PHY devices using a standardised 8 bit ULPI interface, operating at 60MHz.The ULPI interface configuration for the host interfaces is represented in Figure 2-6.

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The host interfaces include a MIC2025USB power switch component, controlled to provide 5V power output to the Dual USB-A style connector on the board.

Please refer to the device data sheet of the ISP1504A device for further information.
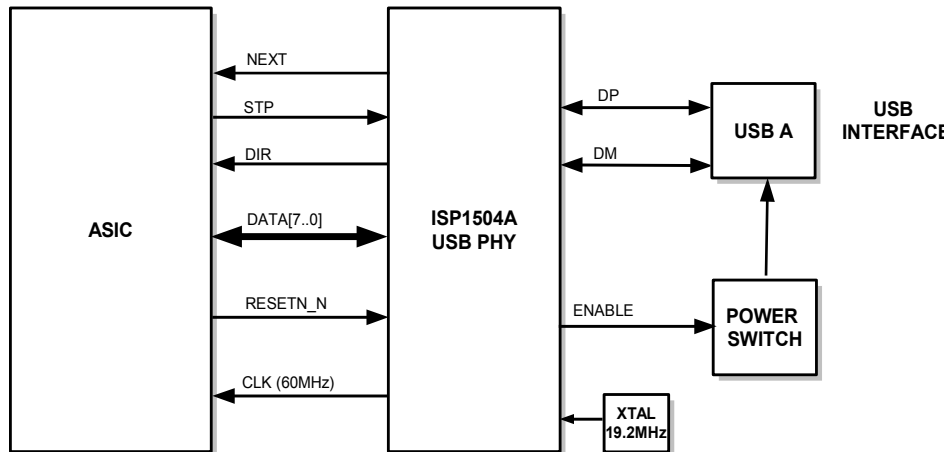
Figure 2-6: USB Host Controller PHYsical Interface

2.7 USB Device

The *LEON4* ASIC device also includes USB 2.0 Device interface, also connected to an ISP1504 USB PHY device on the board, with a 8 bit ULPI interface, operating at 60MHz.

The interface configuration is similar to that represented in Figure 2-6, except that a USB-B device connector is installed on the board, and no power switch is required for this interface

2.8 USB Debug Communication Link

A second USB Device link is provided on the board (Connector J6), which is dedicated for the USB Debug Communication link as described in section 2.17 and section 3.

Note that, to enable this interface, it is necessary that the GPIO43 pin is pulled high at power on of the board.

This can be achieved by inserting a jumper on the pins 17-18 of the header connector J10.

2.9 Video

The *GR-LEON4-ITX* board incorporates an Chrontel CH7301C display controller device for DVI interfaces, providing both Analog and Digital display interfaces on a standard DVI-I style connector.

The LEON4 ASIC incorporates a SVGA controller core with DVI support which interfaces to the controller device to provide a graphical video interface to the board.
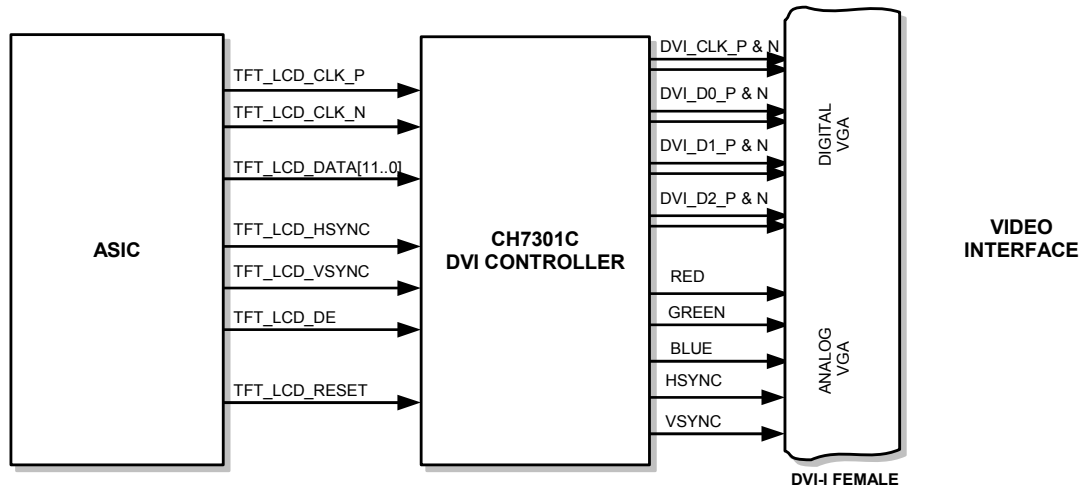
Figure 2-7: DVI Video Interface

2.10 PS2 Keyboard/Mouse Interface

The *GR-LEON4-ITX* board provides two PS2 style interfaces with a standard PS/2 style connector as represented in the figure below, and the logic inside the ASIC provides controller cores for standard PS2 style a Mouse and Keyboard connections.

According the normal conventions for this interface, the top connector (green) is the Mouse interface and the bottom connector (purple) is the Keyboard interface.
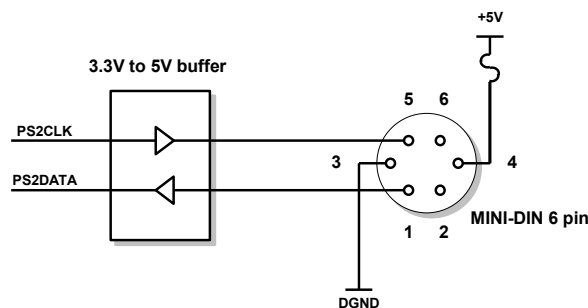
Figure 2-8: PS/2 Interfaces

(one of 2 interfaces shown)

2.11 Serial Interface (RS232)

The *GR-LEON4-ITX-BOARD*, provides RS232 interface circuits and 10 pin headers for two Serial interfaces with TXD/RXD pins.

The RS232 transceiver IC's on this board are SN75C3232 devices from Texas Instruments which operate from a single +3.3V power supply.

The layout and pin ordering of the 10 pin headers is designed so that a simple 1-to-1 ribbon cable connection can be made to a 'standard' Female D-Sub 9 pin type connector with a standard pin-out for serial links.
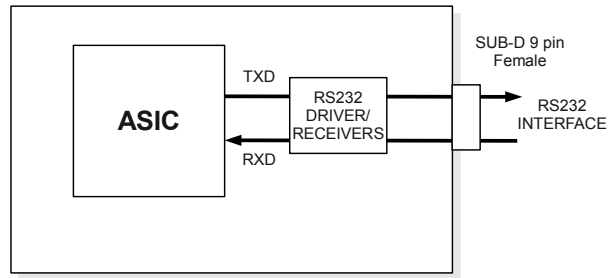
Figure 2-9: Serial interface

The included ribbon cables providing a DE-9 connector should be connected as shown in figure 2-10 (the red stripe should be toward the label UART-1/UART-2).
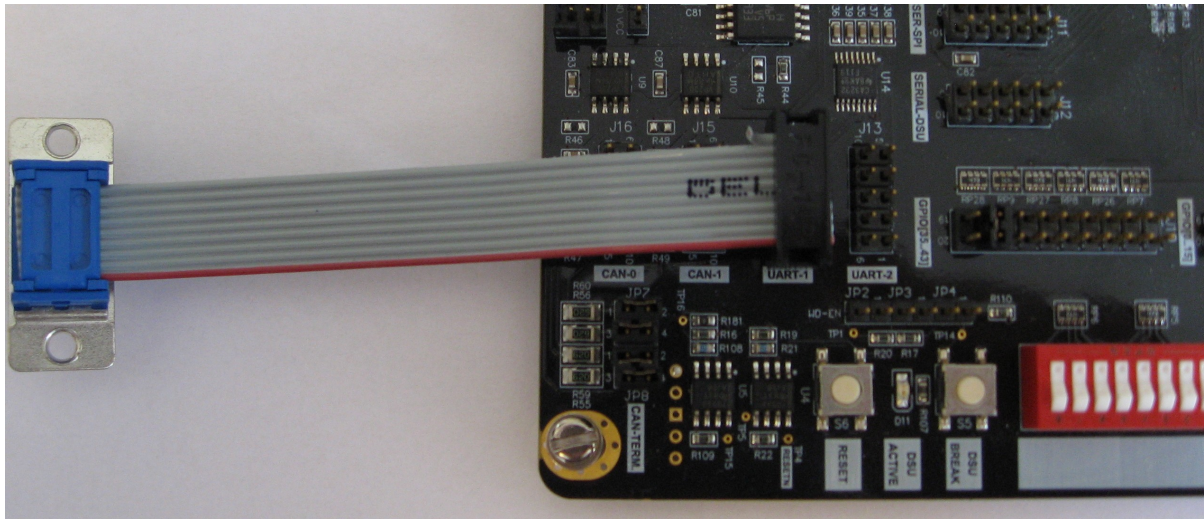
Figure 2-10: Serial interface

2.12 Serial Debug Support Interface (LVTTL)

A 10 pin 0.1" header on the board (J12) provides connections to the serial Debug Support Unit signals DSURX (receive) and DSUTX (transmit).

Note that these voltage levels are 3.3V LVTTL and not RS232 levels. If you wish to connect to this interface would be necessary use an adapter circuit to convert the signals to RS232 levels, or alternatively, a converter chip such as the FTDI FT232 could be used to provide a Serial to USB conversion.

2.13 CAN Interface

The board provides the electrical interfaces for two CAN bus interfaces, as represented in the block diagram, Figure 2-11.

The CAN bus transceiver IC's on this board are *SN65HVD230* devices from Texas Instruments which operate from a single +3.3V power supply.
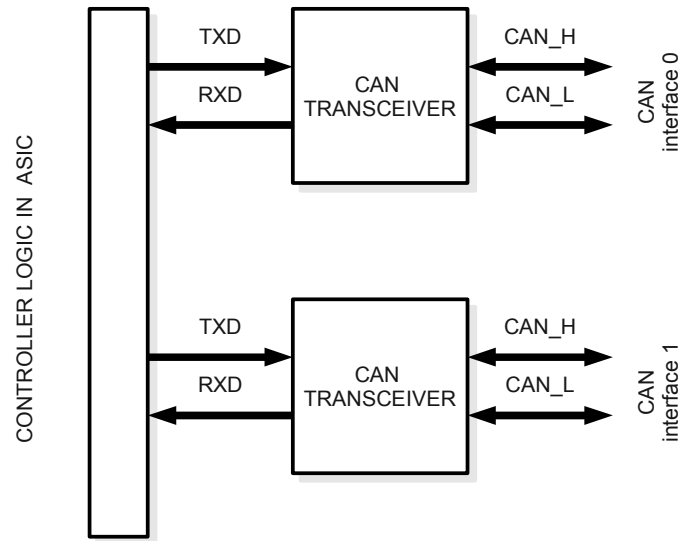
Figure 2-11: Block Diagram of the CAN interface

Configuration of Bus Termination

The CAN interfaces on the board can be configured for either end node or stub-node operation by means of the jumpers JP8 and JP7 for interface 0 and 1 respectively, as shown in Figure 2-12.

For normal end-node termination with a nominal 120 Ohm insert jumpers in position 1-3.

However, if a split termination is desired (if required for improved EMC performance), insert the jumpers in positions 1-2 and 3-4.

For stub nodes, if termination is not required, do not install any jumpers.
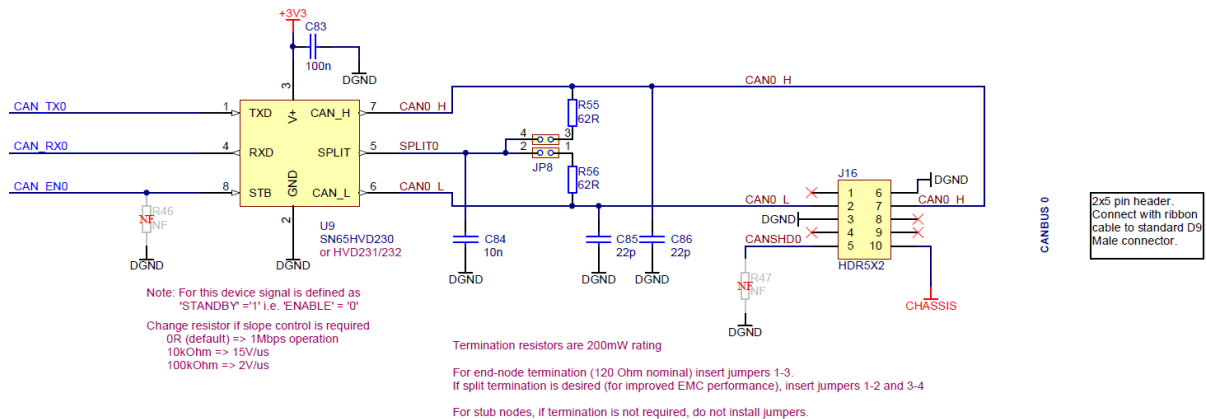
Figure 2-12: Transceiver and Termination Configuration

(one of 2 interfaces shown)

Configuration of Slew Rate

The SN65HVD230 transceiver device used on the board has the facility to set the device into *STANDBY* mode, by connecting an active high external signal to pin 8 of the device. On this board, this pin is connected to the CAN_ENable contorl pin of the ASIC.

A further feature provided by the SN65HVD230 device is the capability to adjust the transceiver slew rate. This can be done by modifying the values of resistors connected to pin 8 of the transceivers.

The default value of 0 ohms is compatible with 1Mbps operation.

From the data sheet the following resistor values give the following slew rates:

   10kOhm => 15V/us

   100kOhm => 2V/us

2.14 I2C interface

The *LEON4 ASIC* device provides three I2C interfaces, two master interfaces (*I2CM0* & *I2CM1*) and one slave interface (I2CS), as shown in Figure 2-13.

As a demonstration I2C circuit, an on-board DS1672 Real-Time Clock circuit is connected on the board to the *I2CM0* interface of the ASIC.

The *I2CM1* and *I2CS* interfaces of the ASIC are connected to 4 pin 0.1" headers on the board, to allow an external circuit to be hooked-up. If required, 10kOhm pull-up resistors on the SCL and SDA signals can be installed if the appropriate jumpers JP9 and JP10 are installed.
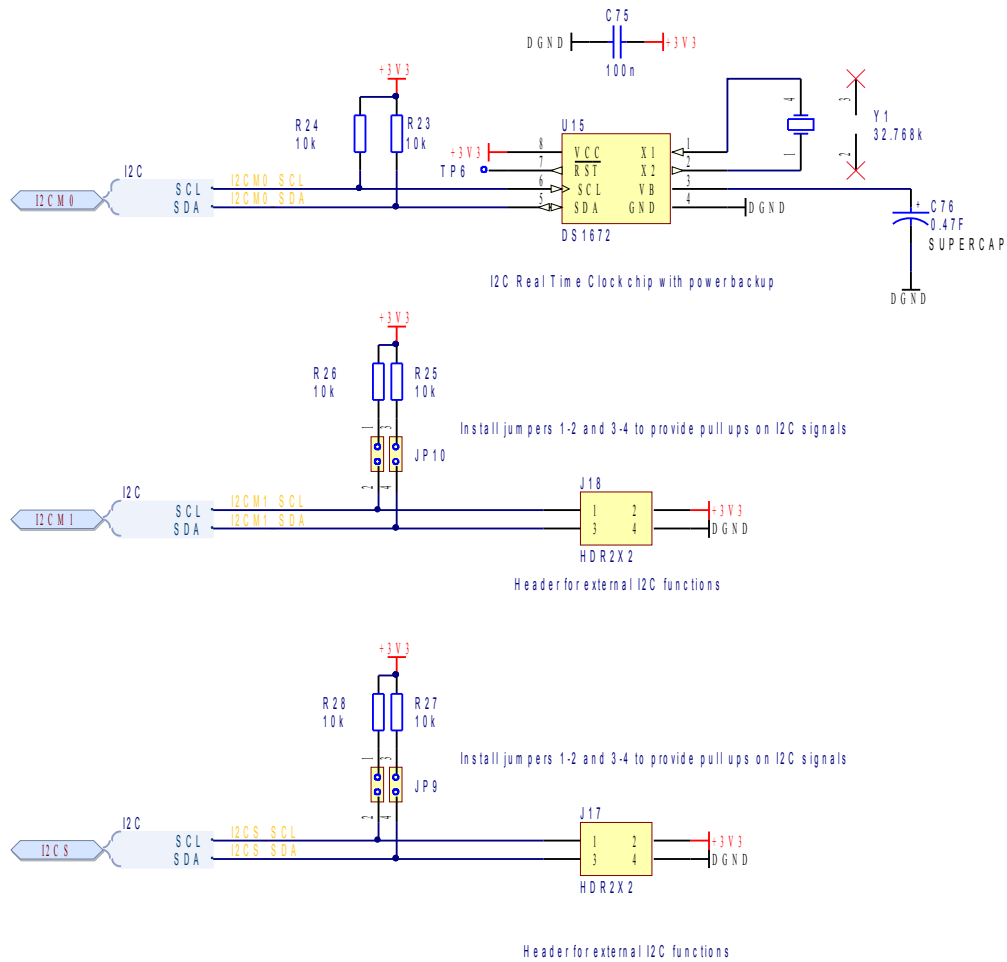
Figure 2-13: I2C Interface Configuration

2.15 SPI interface

In addition to the *SPIM* memory interface (ref section), the *LEON4 ASIC* also provides an SPI interface for user defined devices.

As shown in Figure 2-14 , the SPI interface pins of the *LEON4 ASIC* are connected to an 10 pin 0.1" header on the board to allow an external circuit SPI circuits to be hooked-up.

As an example SPI circuit, the *GR-LEON4-ITX* Board provides an AD7841, Temperature monitor circuit on the board, which is selected with the *SPIC_CS0* output of the ASIC.
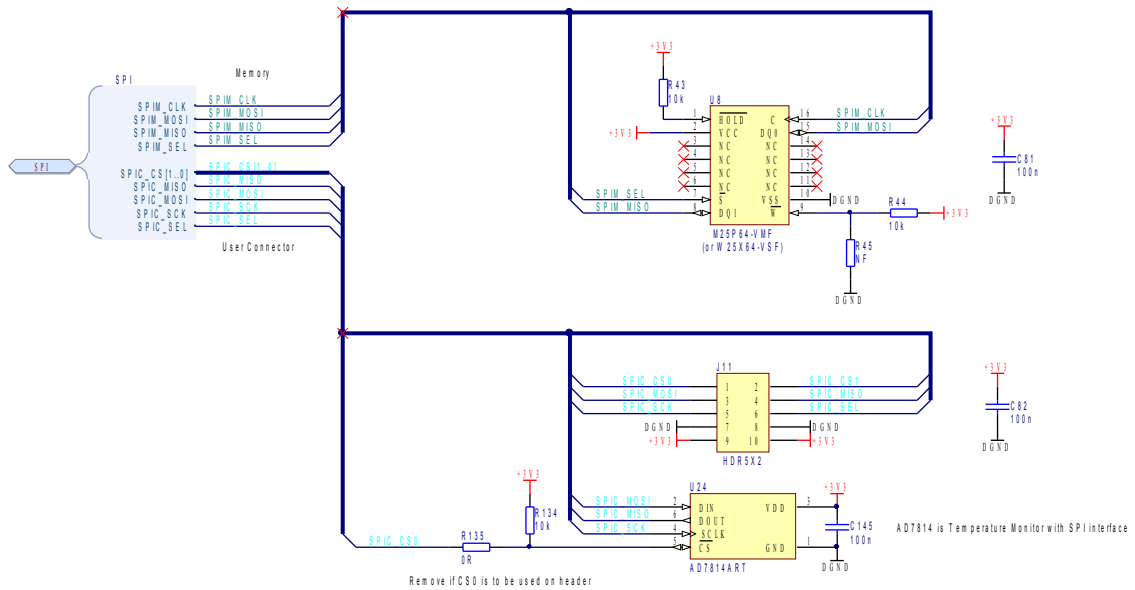
Figure 2-14: SPI Interface Configuration

2.16 GPIO

The *LEON4* ASIC provides 44 general Purpose Input Output signals (3.3V LVTTL voltage levels).

On this board, to provide a range of possible uses, these signals have been connected as follows:

- 25 signals I/O's on 0.1" pin headers
  (with pull-up and series current limiting resistors as shown in Figure 2-15)
- 8 signal inputs on DIP switch S4 (GPIO[23:16])
  (logic '1' input when switch is 'open', else logic '0' when switch is 'closed/on')
- 3 signal inputs on Push button switches (S1, S2, S3) (GPIO[24:26])
  (logic '0' input when pressed, else logic '1')
- 8 signal outputs connected to LED indicators (D3 to D10) (GPIO[27:34])
  ('on' when output is logic '1')
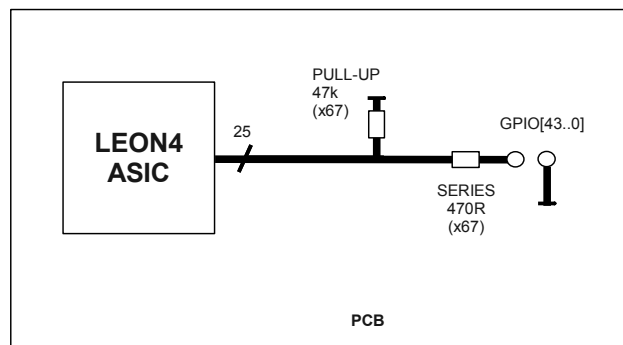
Figure 2-15: PIO interface configuration

2.17 Debug Support Unit Interfaces

Program download and debugging to the processor is performed using the GRMON Debug Monitor tool from Aeroflex Gaisler (RD-5). The *LEON4 ASIC* provides a interface for Debug and control of the processor by means of a host terminal via its DSU interface, as represented in Figure 2-16.
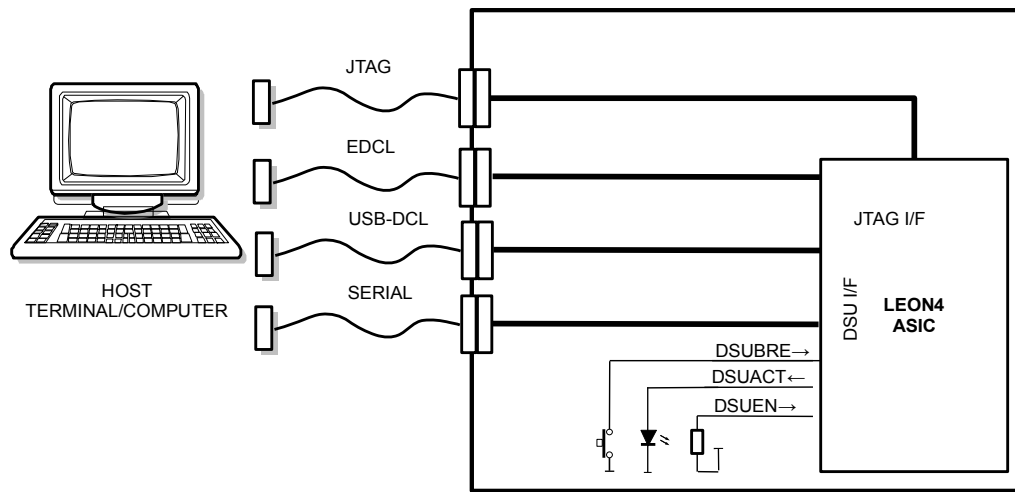
Figure 2-16: Debug Support Unit connections

Three control signals and a data connection form the Debug Support Unit interface to the processor:

DSUEN: This signal is pulled high on the board to enable Debugging

DSUBRE: The push-button forces the processor to halt and enter DSU mode.

DSUACT: When the processor is halted, the LED will illuminate

To communicate with the processor, four possibilities for the data connection to the processor are provided:

SERIAL DSU Serial Debug Communication Link (connector J12)

JTAG-DCL   JTAG Debug Communication Link (connector J19 or J20)

USB-DCL   USB Debug Communication Link (connector J6)

EDCL   Ethernet Debug Communication Link (connector J3)

GRMON can be used with the above listed interfaces, for more information, please refer to RD-5 and RD-6.

2.18 Other Auxiliary Interfaces and Circuits

Oscillators and Clock Inputs

The oscillator and clock scheme for the GR-LEON4-ITX Board is shown in Figure 2-17.

The main oscillator for the *GR-LEON4-ITX* ASIC is a 50 MHz Crystal oscillator. This oscillator is an SMD oscillator soldered on to the board and a zero-delay buffer circuit (CY2305) is used to distribute this 50MHz clock signal.

Addtionally, oscillators are provided as follows:

- 33.3 MHz oscillator with zero delay buffer for PCI interface and slots
- 19.2 MHz, generates 60MHz clock for USB interfaces
- 32.768 kHz crystal for real-time clock chip with battery back-up

Internally to the ASIC, PLL circuits generate the required clock frequencies and phases as represented in Figure 2-18 for the following:

- Processor Main frequency
- DDR2 memory clocks
- Vide Interface clocks
- IP core clocks

If a different user defined main operating frequency of the ASIC is required, this can be achieved by installing a 4 pin DIL8 style oscillator, in socket X2 on the board and moving jumper JP1.
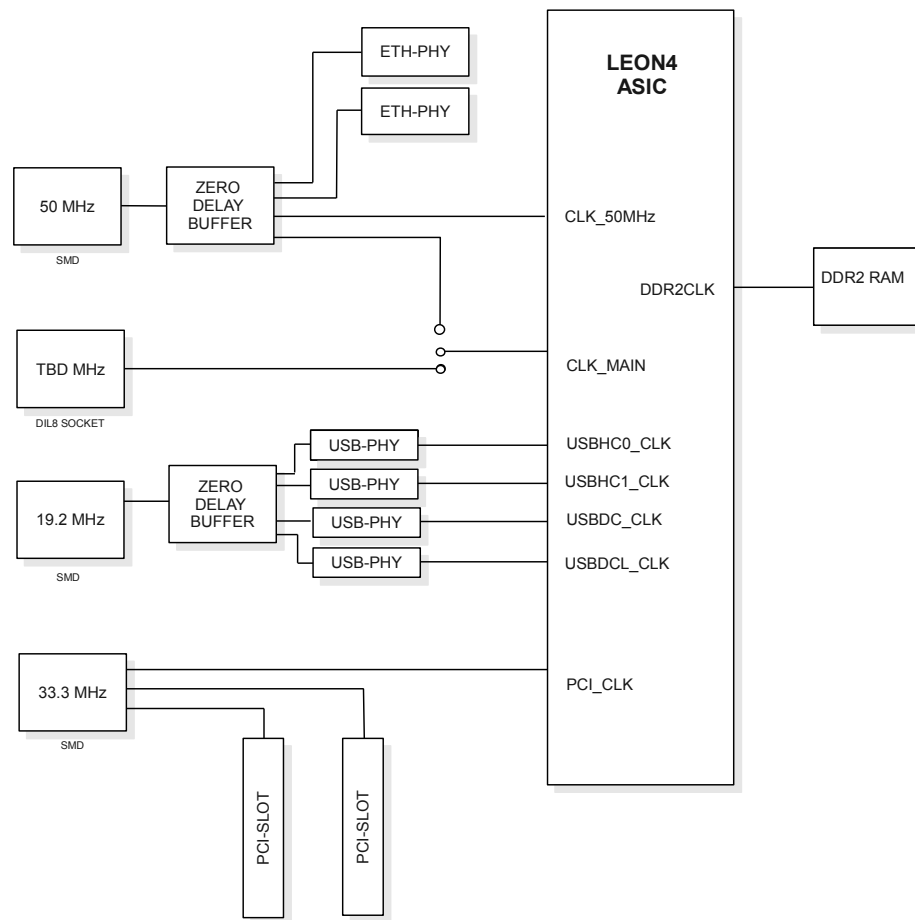
Figure 2-17: Board level Clock Distribution Scheme
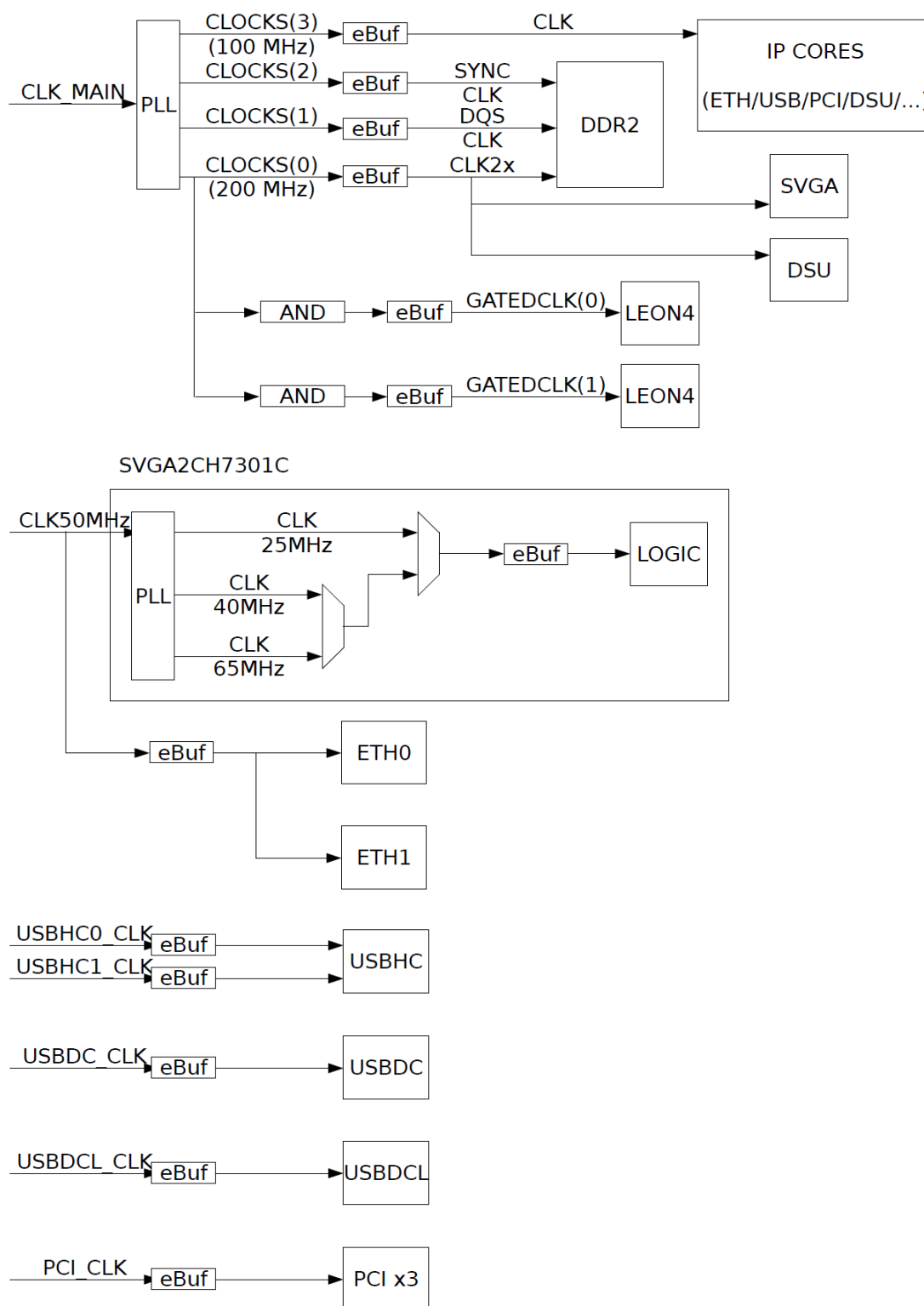
Figure 2-18: Clock and PLL organisation inside LEON4 ASIC

Power Supply and Voltage Regulation

The board operates from a single +5V DC power supply input. On board regulators generate the following voltages:

- +3.3V for the GR-LEON4-ITX I/O voltage, interfaces and other peripherals
- +2.5V for LEON4 configuration voltage
- +1.8V for DDR2 supply voltage
- +1.2V for LEON4 Vcore voltage
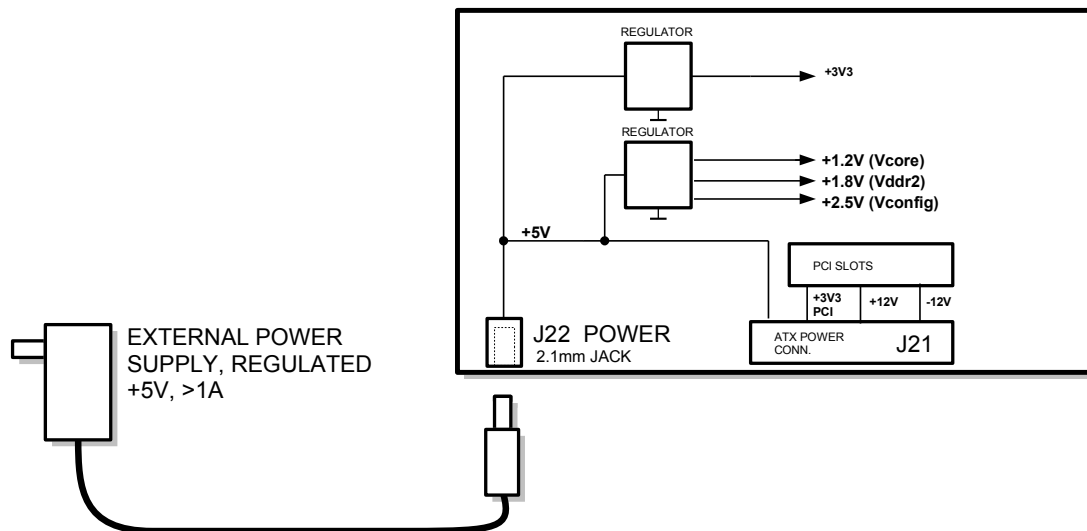
Figure 2-19: Power Regulation Configuration

As an alternative to the single +5V power supply input, an ATX style power connector is also provided on the board, which may be more convenent if the board is to be installed in a Mini-ITX style housing.

If PCI slots are to be used, then the ATX power connector should be used in order that +3.3V, +5V, +12V and -12V will be correctly provided to the peripheral cards installed in the slots.

Reset Circuit and Button

A standard Processor Power Supervisory circuit (TPS3705 or equivalent) is provided on the Board to provide monitoring of the 3.3V power supply rail and to generate a clean reset signal at power up of the Unit.

To provide a manual reset of the board, a miniature push button switch is provided on the Main PCB for the control. Additionally connections are provided to an additional off-board push-button *RESET* switch if this is required.

Watchdog

The *LEON4* ASIC includes a Watchdog timer function which can be used for the purpose of generating a system reset in the event of a software malfunction or crash.

On this development board the *WDOGN* signal is connected as shown in the Figure 2-20 to

the Processor Supervisory circuit.
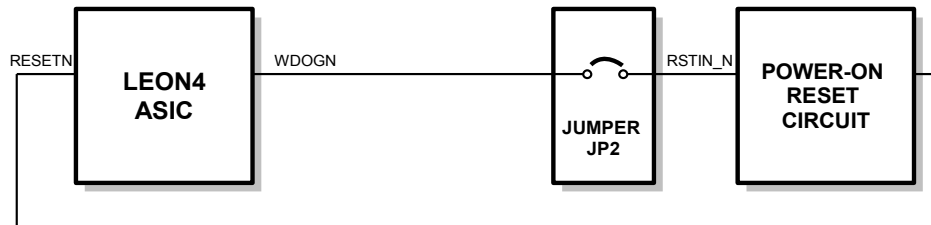
Figure 2-20: Watchdog configuration

To utilise the Watchdog feature, it is necessary to appropriately set-up and enable the Watchdog timer. Please consult the *LEON4 ASIC* data sheet (RD-4) for the correct register locations and details.

Also, to allow the *WDOGN* signal to generate a system reset it is necessary to install the Jumper JP2 (see Figure 2-20).

For software development it is often convenient or necessary to disable the Watchdog triggering in order to be able to easily debug without interference from the Watchdog operation. In this case, the Jumper JP2 should be *removed*. When the watchdog triggers, a system reset will not occur.

JTAG interface

Two connectors on the back edge of the PCB provide the possibility to connect to the JTAG signals and JTAG chain of the *LEON4* ASIC.

This interface allows DSU Debug over the JTAG interface to be performed.

Two connectors are provided, J20, a 14 pin 2mm Molex connector for connection with ribbon cable to a JTAG cable such as the Xilinx Parallel IV or Platform USB cable, and J19, which is a 6 pin 0.1" header which can be used to connect to Parallel III style cables.

eASIC SPI Configuration Interface

In order to store configuration bit information for the EASIC structured ASIC a dedicated SPI PROM (U2) is provided on the board with its own 6 pin header for programming (J24).

This configuration information is automatically read out of the PROM by the ASIC when the board is powered up in order to bring the ASIC into full operation.

When programming the SPI Configuration Prom, the jumpers JP11 must be removed in order to 'disconnect' the prom form the ASIC. In normal use the jumpers JP11 should be installed 1-2, 3-4, 5-6, 7-8 so that the correct communication can occur between the ASIC and PROM.

The configuration prom will normally be pre-programmed during manufacture/test of the board, and since these parameters are not user accessible, the functioning and programming of this prom are not further described in this document.

3   SETTING UP AND USING THE BOARD

The default status of the Jumpers on the boards is as shown in Table 3-1.

For the meaning of the various jumpers, refer to Table 4-3 and RD 1.

Jumper	Jumper Setting	Comment
JP1	Installed 1-2	Connects 50MHz Main Oscillator for main CLK
J10	Installed 17-18	This inserts a pull-up on GPIO43 to enable USB-DCL on power up.
JP11	Installed 1-2, 3-4, 5-6, 7-8	

Table 3-1: Default Status of Jumpers/Switches

To operate the unit stand alone on the bench top, connect the +5V power supply to the Power Socket J22 at the back of the unit.

The POWER LED should be illuminated indicating that the +3.3V power is active.

Upon power on, the Processor will start executing instructions beginning at the memory location 0x00000000, which is the start of the PROM. If the PROM is 'empty' or no valid program is installed, the first executed instruction will be invalid, and the processor will halt with an ERROR condition, with the ERROR LED illuminated.

To perform program download and software debugging on the hardware it is necessary to use the Gaisler Research *GRMON* debugging software, installed on a host PC (as represented in Figure 2-16). Please refer to the *GRMON* documentation for the installation of the software on the host PC (Linux or Windows), and for the installation of the associated hardware dongle.

To perform software download and debugging on the processor, a link from the Host computer to the DSU interface of the board is necessary. As described in section 2.17 there are four possible DSU interfaces available on this board:

  SERIAL DSU   Serial Debug Communication Link (connector J12)

  JTAG-DCL   JTAG Debug Communication Link (connector J19 or J20)

  USB-DCL   USB Debug Communication Link (connector J6)

  EDCL   Ethernet Debug Communication Link (connector J3)

Program download and debugging can be performed in the usual manner with *GRMON.* More information on the usage, commands and debugging features of *GRMON,* is given in the *GRMON Users Manual* and associated documentation. The *GR-LEON4-ITX Quick Start Guide* contains more information and examples on using the board.

4   INTERFACES AND CONFIGURATION

4.1 List of Connectors

| Name	Function	Type	Description
PCI-J1	PCI Slot 0	AMP 5145098-1	120 pin (32 bit) PCI motherboard interface – slot 0
PCI-J2	PCI Slot 1	AMP 5145098-1	120 pin (32 bit) PCI motherboard interface – slot 1
J3A	ETHERNET-1	Dual RJ45-Top	10/100Mbit/s Ethernet Connector 1
J3B	ETHERNET-0	Dual RJ45-Bottom	10/100Mbit/s Ethernet Connector 0
J4A	USB-HOST 0	Dual USB-A Top	USB Host Interface - 0
J4B	USB-HOST 1	Dual USB-A Bottom	USB Host Interface - 1
J5	USB-DEVICE	USB-B	USB Device interface
J6	USB-DCL	USB-B	USB Debug link interface
J7	DVI Video	MOLEX 74320-1004	DVI-I (Analog and Digital) Video Interface
J8A	MOUSE	Dual PS2-Top	PS2 Keyboard interface
J8B	KEYBOARD	Dual PS2-Bottom	PS2 Mouse interface
J9	GPIO[15..0]	20 pin 0.1" Header	Pin connections for PIO signals 0 to 15
J10	GPIO[43..35]	20 pin 0.1" Header	Pin connections for PIO signals 35 to 43
J11	SPI	10 pin 0.1" Header	Header for User SPI interface
J12	UART-DSU	10 pin 0.1" Header	Header for Serial DSU signals
J13	UART-2	10 pin 0.1" Header	Header for Serial UART2 signals
J14	UART-1	10 pin 0.1" Header	Header for Serial UART 1 signals
J15	CAN-1	10 pin 0.1" Header	Header for CANBUS-1 signals
J16	CAN-0	10 pin 0.1" Header	Header for CANBUS-0 signals
J17	I2C Slave	4 pin 0.1" Header	Pin connections for User I2C interface
J18	I2C Master1	4 pin 0.1" Header	Pin connections for User I2C interface
J19	JTAG-DSU	6 pin 0.1" Header	JTAG signal interface for DSU
J20	JTAG-DSU	2x7pin 2mm header	JTAG signal interface for DSU
J21	POWER_ATX	MOLEX 39-29-9202	ATX Style power input connector
J22	POWER_5V	2.1mm centre +ve	+5V DC power input connector
J23	JTAG-ASIC	6 pin 0.1" Header	ASIC JTAG interface
J24	PROM-PROG	6 pin 0.1" Header	Config Prom SPI program interface

Table 4-1: List of Connectors
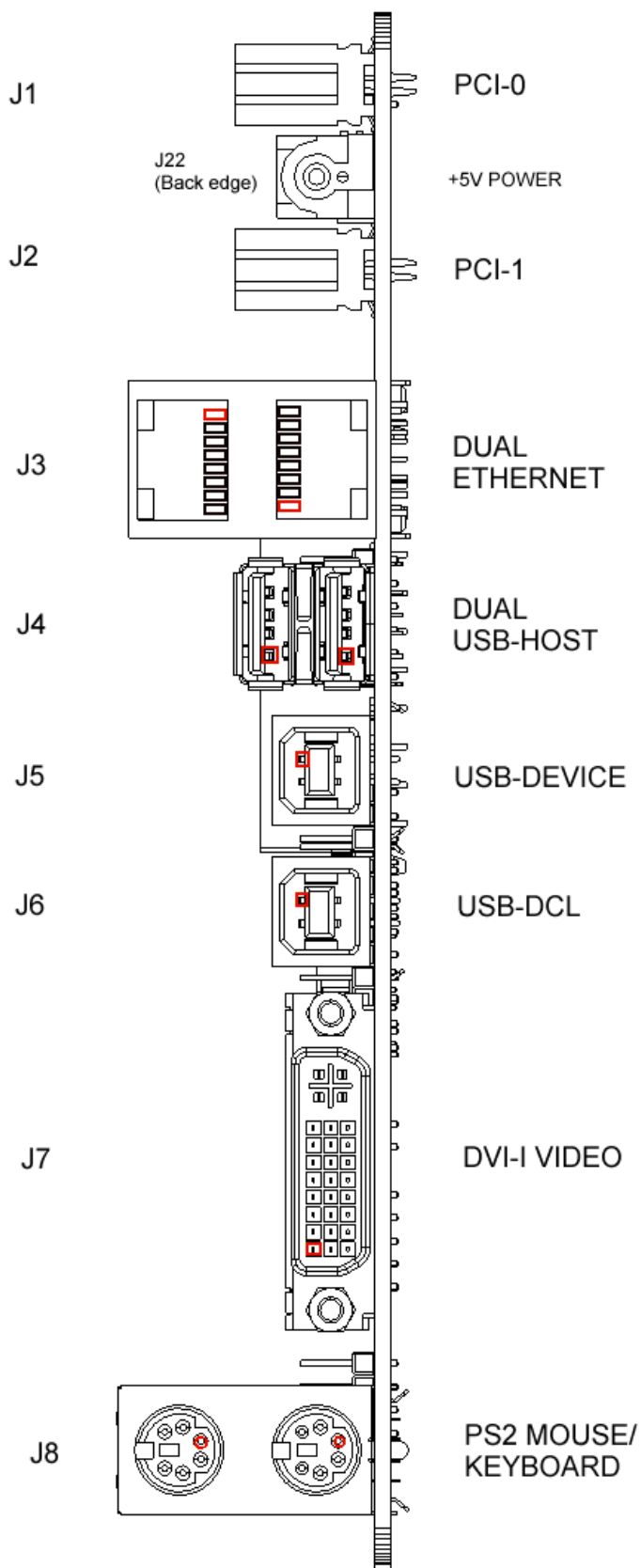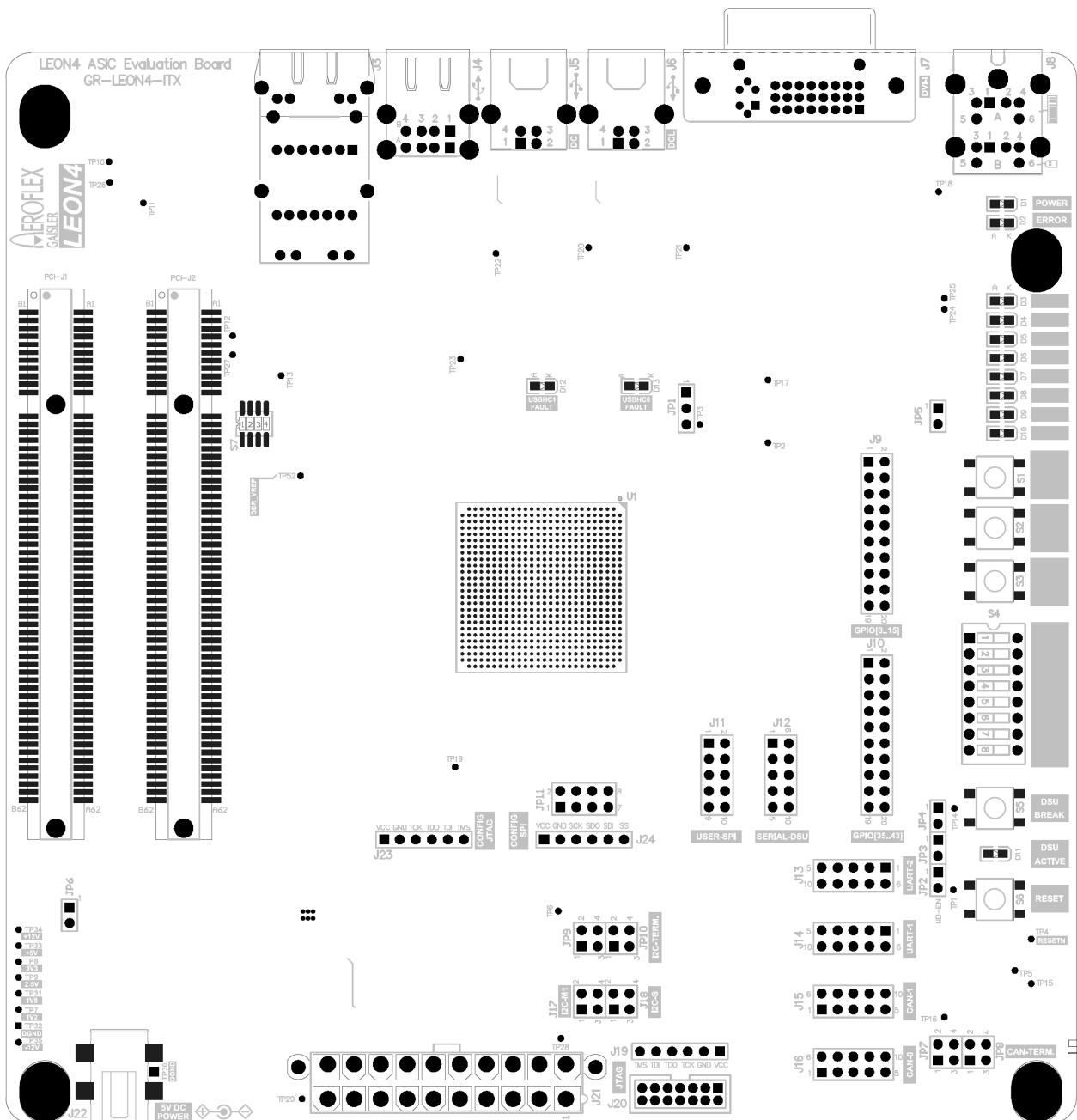
Figure 4-1: Front Panel View (pin 1 of connectors marked)

Figure 4-2: Board Connector View

PCI-J1

Left Net	B Pin	B Signal	A Signal	A Pin	Right Net
-12V	B1	-12V	TRST#/NC	A1	PCI_TRST
PCI_TCK	B2	TCK/NC	+12V	A2	+12V
DGND	B3	GROUND	TMS/NC	A3	PCI_TMS
	B4	TDO/NC	TDI/NC	A4	PCI_TDI
+5V	B5	+5V	+5V	A5	+5V
+5V	B6	+5V	INTA#	A6	PCI_INTA
PCI_INTB	B7	INTB#	INTC#	A7	PCI_INTC
PCI_INTD	B8	INTD#	+5V	A8	+5V
	B9	PRSNT1#/NC	RES./CLKC	A9	
	B10	RES./REQ1#	+VI/O(3.3V)	A10	+3V3PCI
	B11	PRSNT2#/NC	RESERVED	A11	
	B14	RES./GNT1#	RES./CLKA	A14	
DGND	B15	GROUND	RST#	A15	PCI_RST
PCI_CLKA	B16	CLK/CLKB	+VI/O(3.3V)	A16	+3V3PCI
DGND	B17	GROUND	GNT#/GNT0#	A17	PCI_ARB_GNT0
PCI_ARB_REQ0	B18	REQ#/REQ0#	GROUND	A18	DGND
	B19	+VI/O(3.3V)	RES./REQ2#	A19	
PCI_AD31	B20	AD[31]	AD[30]	A20	PCI_AD30
PCI_AD29	B21	AD[29]	+3V3/NC	A21	+3V3PCI
DGND	B22	GROUND	AD[28]	A22	PCI_AD28
PCI_AD27	B23	AD[27]	AD[26]	A23	PCI_AD26
PCI_AD25	B24	AD[25]	GROUND	A24	DGND
PCI_CBE3 / +3V3PCI	B25	+3V3/NC	AD[24]	A25	PCI_AD24
PCI_AD23	B26	C/BE[3]#	IDSEL/GNT2#	A26	PCI_AD16
	B27	AD[23]	+3V3/NC	A27	+3V3PCI
DGND	B28	GROUND	AD[22]	A28	PCI_AD22
PCI_AD21	B29	AD[21]	AD[20]	A29	PCI_AD20
PCI_AD19	B30	AD[19]	GROUND	A30	DGND
PCI_AD17 / +3V3PCI	B31	+3V3/NC	AD[18]	A31	PCI_AD18
	B32	AD[17]	AD[16]	A32	PCI_AD16
PCI_CBE2	B33	C/BE[2]#	+3V3/NC	A33	+3V3PCI
DGND	B34	GROUND	FRAME#	A34	PCI_FRAME
PCI_IRDY	B35	IRDY#	GROUND	A35	DGND
PCI_DEVSEL / +3V3PCI	B36	+3V3/NC	TRDY#	A36	PCI_TRDY
	B37	DEVSEL#	GROUND	A37	DGND
PCI_LOCK / DGND	B38	GROUND	STOP#	A38	PCI_STOP
PCI_PERR	B39	LOCK#	+3V3/NC	A39	+3V3PCI
	B40	PERR#	SDONE	A40	
PCI_SERR / +3V3PCI	B41	+3V3/NC	SBO#	A41	
	B42	SERR#	GROUND	A42	DGND
PCI_CBE1 / +3V3PCI	B43	+3V3/NC	PAR	A43	PCI_PAR
PCI_AD14	B44	C/BE[1]#	AD[15]	A44	PCI_AD15
	B45	AD[14]	+3V3/NC	A45	+3V3PCI
PCI_AD12 / DGND	B46	GROUND	AD[13]	A46	PCI_AD13
PCI_AD10	B47	AD[12]	AD[11]	A47	PCI_AD11
	B48	AD[10]	GROUND	A48	DGND
	B49	M66EN/GND	AD[09]	A49	PCI_AD9
PCI_AD8	B52	AD[08]	C/BE[0]#	A52	PCI_CBE0
PCI_AD7	B53	AD[07]	+3V3/NC	A53	+3V3PCI
PCI_AD5 / +3V3PCI	B54	+3V3/NC	AD[06]	A54	PCI_AD6
PCI_AD3	B55	AD[05]	AD[04]	A55	PCI_AD4
	B56	AD[03]	GROUND	A56	DGND
PCI_AD1 / DGND	B57	GROUND	AD[02]	A57	PCI_AD2
	B58	AD[01]	AD[00]	A58	PCI_AD0
PCI_ACK64N / +3V3PCI	B59	+VI/O(3.3V)	+VI/O(3.3V)	A59	+3V3PCI
	B60	ACK64#	REQ64#/NC	A60	PCI_REQ64N
+5V	B61	+5V	+5V	A61	+5V
+5V	B62	+5V	+5V	A62	+5V

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Table 4-2: PCI-J1 PCI Connector Slot 0

PCI-J2

Net (B)	B pin	B signal	A signal	A pin	Net (A)
-12V	B1	-12V	TRST#/NC	A1	PCI_TRST
PCI_TCK	B2	TCK/NC	+12V	A2	+12V
DGND	B3	GROUND	TMS/NC	A3	PCI_TMS
	B4	TDO/NC	TDI/NC	A4	PCI_TDI
+5V	B5	+5V	+5V	A5	+5V
+5V	B6	+5V	INTA#	A6	PCI_INTB
PCI_INTC	B7	INTB#	INTC#	A7	PCI_INTD
PCI_INTA	B8	INTD#	+5V	A8	+5V
	B9	PRSNT1#/NC	RES./CLKC	A9	
	B10	RES./REQ1#	+VI/O(3.3V)	A10	+3V3PCI
	B11	PRSNT2#/NC	RESERVED	A11	
	B14	RES./GNT1#	RES./CLKA	A14	
DGND	B15	GROUND	RST#	A15	PCI_RST
PCI_CLKB	B16	CLK/CLKB	+VI/O(3.3V)	A16	+3V3PCI
DGND	B17	GROUND	GNT#/GNT0#	A17	PCI_ARB_GNT1
PCI_ARB_REQ1	B18	REQ#/REQ0#	GROUND	A18	DGND
+3V3PCI	B19	+VI/O(3.3V)	RES./REQ2#	A19	
PCI_AD31	B20	AD[31]	AD[30]	A20	PCI_AD30
PCI_AD29	B21	AD[29]	+3V3/NC	A21	+3V3PCI
DGND	B22	GROUND	AD[28]	A22	PCI_AD28
PCI_AD27	B23	AD[27]	AD[26]	A23	PCI_AD26
PCI_AD25	B24	AD[25]	GROUND	A24	DGND
+3V3PCI	B25	+3V3/NC	AD[24]	A25	PCI_AD24
PCI_CBE3	B26	C/BE[3]#	IDSEL/GNT2#	A26	PCI_AD17
PCI_AD23	B27	AD[23]	+3V3/NC	A27	+3V3PCI
DGND	B28	GROUND	AD[22]	A28	PCI_AD22
PCI_AD21	B29	AD[21]	AD[20]	A29	PCI_AD20
PCI_AD19	B30	AD[19]	GROUND	A30	DGND
+3V3PCI	B31	+3V3/NC	AD[18]	A31	PCI_AD18
PCI_AD17	B32	AD[17]	AD[16]	A32	PCI_AD16
PCI_CBE2	B33	C/BE[2]#	+3V3/NC	A33	+3V3PCI
DGND	B34	GROUND	FRAME#	A34	PCI_FRAME
PCI_IRDY	B35	IRDY#	GROUND	A35	DGND
+3V3PCI	B36	+3V3/NC	TRDY#	A36	PCI_TRDY
PCI_DEVSEL	B37	DEVSEL#	GROUND	A37	DGND
DGND	B38	GROUND	STOP#	A38	PCI_STOP
PCI_LOCK	B39	LOCK#	+3V3/NC	A39	+3V3PCI
PCI_PERR	B40	PERR#	SDONE	A40	
+3V3PCI	B41	+3V3/NC	SBO#	A41	
PCI_SERR	B42	SERR#	GROUND	A42	DGND
+3V3PCI	B43	+3V3/NC	PAR	A43	PCI_PAR
PCI_CBE1	B44	C/BE[1]#	AD[15]	A44	PCI_AD15
PCI_AD14	B45	AD[14]	+3V3/NC	A45	+3V3PCI
DGND	B46	GROUND	AD[13]	A46	PCI_AD13
PCI_AD12	B47	AD[12]	AD[11]	A47	PCI_AD11
PCI_AD10	B48	AD[10]	GROUND	A48	DGND
	B49	M66EN/GND	AD[09]	A49	PCI_AD9
PCI_AD8	B52	AD[08]	C/BE[0]#	A52	PCI_CBE0
PCI_AD7	B53	AD[07]	+3V3/NC	A53	+3V3PCI
+3V3PCI	B54	+3V3/NC	AD[06]	A54	PCI_AD6
PCI_AD5	B55	AD[05]	AD[04]	A55	PCI_AD4
PCI_AD3	B56	AD[03]	GROUND	A56	DGND
DGND	B57	GROUND	AD[02]	A57	PCI_AD2
PCI_AD1	B58	AD[01]	AD[00]	A58	PCI_AD0
+3V3PCI	B59	+VI/O(3.3V)	+VI/O(3.3V)	A59	+3V3PCI
PCI_ACK64N	B60	ACK64#	REQ64#/NC	A60	PCI_REQ64N
+5V	B61	+5V	+5V	A61	+5V
+5V	B62	+5V	+5V	A62	+5V

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Table 4-3: PCI-J2 PCI Connector Slot 1

Pin	Name	Comment
1	TPFOP	Output +ve
2	TPFON	Output -ve
3	TPFIP	Input +ve
4	TPFOC	Output centre-tap
5		No connect
6	TPFIN	Input -ve
7	TPFIC	Input centre-tap
8		No connect

Table 4-4: J3A (Top) RJ45 10/100Mbit/s Ethernet Connector 1

Pin	Name	Comment
1	TPFOP	Output +ve
2	TPFON	Output -ve
3	TPFIP	Input +ve
4	TPFOC	Output centre-tap
5		No connect
6	TPFIN	Input -ve
7	TPFIC	Input centre-tap
8		No connect

Table 4-5: J3B (Bottom) RJ45 10/100Mbit/s Ethernet Connector 0

Pin	Name	Comment
1	VBUS	+5V (to external device)
2	DM	Data Minus
3	DP	Data Plus
4	DGND	Ground

Table 4-6: J4A (Top) *USB* type A connector – USB-Host 0

Pin	Name	Comment
1	VBUS	+5V (to external device)
2	DM	Data Minus
3	DP	Data Plus
4	DGND	Ground

Table 4-7: J4B (Bottom) *USB* type A connector – USB-Host 1

Pin	Name	Comment
1	VBUS	+5V (from external host)
2	DM	Data Minus
3	DP	Data Plus
4	DGND	Ground

Table 4-8: J5 *USB* type B connector – USB Device

Pin	Name	Comment
1	VBUS	+5V (from external host)
2	DM	Data Minus
3	DP	Data Plus
4	DGND	Ground

Table 4-9: J6 USB type B connector – USB Debug Communication Link

Pin	Name	Comment
1	Data 2-	Digital red - (Link 1)
2	Data 2+	Digital red + (Link 1)
3	Data 2/4 shield	
4	Data 4-	Digital green - (Link 2) - not connected on this board
5	Data 4+	Digital green + (Link 2) - not connected on this board
6	DDC clock	
7	DDC data	
8	Analog vertical sync	Vsync
9	Data 1-	Digital green - (Link 1)
10	Data 1+	Digital green + (Link 1)
11	Data 1/3 shield	
12	Data 3-	Digital blue - (Link 2) - not connected on this board
13	Data 3+	Digital blue + (Link 2) - not connected on this board
14	+5 V	Power for monitor when in standby
15	Ground	Return for pin 14 and analog sync
16	Hot plug detect	
17	Data 0-	Digital blue - (Link 1) and digital sync
18	Data 0+	Digital blue + (Link 1) and digital sync
19	Data 0/5 shield	
20	Data 5-	Digital red - (Link 2) - not connected on this board
21	Data 5+	Digital red + (Link 2) - not connected on this board
22	Clock shield	
23	Clock+	Digital clock + (Links 1 and 2)
24	Clock-	Digital clock - (Links 1 and 2)
C1	Analog red	Red
C2	Analog green	Green
C3	Analog blue	Blue
C4	Analog horizontal sync	Hsync
C5	Analog ground	Return for R, G and B signals

Table 4-10: J7 DVI-I connector – Video

Pin	Name	ASIC Pin	Comment
1	MOUSE_DATA	E19	Data in
2	nc		No connect
3	DGND		Ground
4	V+		+5V
5	MOUSE_CLK	D19	Clock out
6	nc		No connect

Table 4-11: J8A (Top) PS2 Connector - Mouse

Pin	Name	ASIC Pin	Comment
1	KEYB_DATA	B19	Data in
2	nc		No connect
3	DGND		Ground
4	V+		+5V
5	KEYB_CLK	A19	Clock out
6	nc		No connect

Table 4-12: J8B (Bottom) PS2 Connector – Keyboard

FUNCTION	ASIC pin	CONNECTOR PIN		ASIC pin	FUNCTION
GPIO0	A13	1	2	B13	GPIO1
GPIO2	C13	3	4	D13	GPIO3
GPIO4	E13	5	6	F13	GPIO5
GPIO6	G13	7	8	A12	GPIO7
GPIO8	B12	9	10	D12	GPIO9
GPIO10	E12	11	12	F12	GPIO11
GPIO12	G12	13	14	H12	GPIO13
GPIO14	A11	15	16	B11	GPIO15
+3V3		17	18		+3V3
DGND		19	20		DGND

Table 4-13: J9 - GPIO[15..0] Header connections for PIO signals 0 to 15

FUNCTION	ASIC pin	CONNECTOR PIN		FUNCTION
GPIO35	B8	1	2	DGND
GPIO36	D8	3	4	DGND
GPIO37	F8	5	6	DGND
GPIO38	G8	7	8	DGND
GPIO39	A7	9	10	DGND
GPIO40	B7	11	12	DGND
GPIO41	C7	13	14	DGND
GPIO42	D7	15	16	DGND
GPIO43	E7	17	18	DGND
nc		19	20	DGND

Table 4-14: J10 - GPIO[43..35] Header connections for PIO signals 35 to 43

FUNCTION	ASIC pin	CONNECTOR PIN				ASIC pin	FUNCTION
SPIC_CS0	A24	1	■	□	6	B24	SPIC_CS0
SPIC_MOSI	B23	2	□	□	7	A23	SPIC_MISO
SPIC_SCK	A22	3	□	□	8	C22	SPIC_SEL
DGND		4	□	□	9		DGND
+3V3		5	□	□	10		+3V3

Table 4-15: J11- SPI Header for User SPI interface

FUNCTION	ASIC pin	CONNECTOR PIN				FUNCTION
nc		1	■	□	6	nc
DSUTX	A20	2	□	□	7	nc
DSURX	G21	3	□	□	8	nc
nc		4	□	□	9	nc
DGND		5	□	□	10	CHASSIS

Table 4-16: J12 - UART-DSU Header for Serial DSU signals

FUNCTION	ASIC pin	CONNECTOR PIN				FUNCTION
nc		1	■	□	6	nc
TXD-2	E20	2	□	□	7	nc
RXD-2	C20	3	□	□	8	nc
nc		4	□	□	9	nc
DGND		5	□	□	10	CHASSIS

Table 4-17: J13 – UART-2 Header for Serial UART2 signals

FUNCTION	ASIC pin	CONNECTOR PIN				FUNCTION
nc		1	■	□	6	nc
TXD-1	D20	2	□	□	7	nc
RXD-1	B20	3	□	□	8	nc
nc		4	□	□	9	nc
DGND		5	□	□	10	CHASSIS

Table 4-18: J14 -UART-1 Header for Serial UART 1 signals

FUNCTION	CONNECTOR PIN				FUNCTION
nc	1	■	□	6	DGND
CAN1_L	2	□	□	7	CAN1_H
DGND	3	□	□	8	nc
nc	4	□	□	9	nc
CANSHD	5	□	□	10	CHASSIS

Table 4-19: J15 -CAN-1 Header for CANBUS-1 signals

FUNCTION		CONNECTOR PIN		FUNCTION
nc	1	■ □	6	DGND
CAN0_L	2	□ □	7	CAN0_H
DGND	3	□ □	8	nc
nc	4	□ □	9	nc
CANSHD	5	□ □	10	CHASSIS

Table 4-20: J16 -CAN-0 Header for CANBUS-0 signals

FUNCTION	ASIC pin	CONNECTOR PIN		FUNCTION
I2CS_SCL	F26	1 ■ □	2	+3V3
I2CS_SDA	F24	3 □ □	4	DGND

Table 4-21: J17 -I2C Slave Pin connections for User I2C interface

FUNCTION	ASIC pin	CONNECTOR PIN		FUNCTION
I2CM1_SCL	E24	1 ■ □	2	+3V3
I2CM1_SDA	E23	3 □ □	4	DGND

Table 4-22: J18 -I2C Master1 Pin connections for User I2C interface

Pin	Name	Comment
1	V+	3.3V
2	DGND	Ground
3	TCK	DSU-JTAG: TCK
4	TDO	DSU-JTAG: TDO
5	TDI	DSU-JTAG TDI
6	TMS	DSU-JTAG: TMS

Table 4-23: J19 -Debug Support Unit JTAG signal interface

Pin	Name	Comment
1	DGND	Ground
2	VREF	3.3V
3	DGND	Ground
4	TMS	JTAG: TMS
5	DGND	Ground
6	TCK	JTAG: TCK
7	DGND	Ground
8	TDO	JTAG: TDO
9	DGND	Ground
10	TDI	JTAG: TDI
11	DGND	Ground
12	NC	No connect
13	DGND	Ground
14	NC	No connect

Table 4-24: J20 -JTAG signal interface

Pin	Name	Comment
1	+3V3	Provides 3.3V to PCI slots
2	+3V3	Provides 3.3V to PCI slots
3	DGND	Ground
4	+5V	+5V main supply for board
5	DGND	Ground
6	+5V	+5V main supply for board
7	DGND	Ground
8	POWEROK	Power OK signal from ATX supply (not used)
9	+5VSB	+5V stand-by power (not used)
10	+12V	Provides +12V to PCI slots
11	+3V3	Provides 3.3V to PCI slots
12	-12V	Provides -12V to PCI slots
13	DGND	Ground
14	POWERON	Power on signal to ATX Supply (strapped to DGND on board)
15	DGND	Ground
16	DGND	Ground
17	DGND	Ground
18	-5V	-5V from ATX power supply (not used)
19	+5V	+5V main supply for board
20	+5V	+5V main supply for board

Table 4-25: J21 -POWER - ATX Style power input connector

Pin	Name	Comment
+VE	+5V	Inner Pin, 5V, typically TBD A
-VE	GND	Outer Pin Return

Table 4-26: J22 -POWER +5V DC power input connector

Pin	Name	Comment
1	V+	3.3V
2	DGND	Ground
3	TCK	JTAG: TCK
4	TDO	JTAG: TDO
5	TDI	JTAG TDI
6	TMS	JTAG: TMS

Table 4-27: J23 -ASIC-JTAG JTAG interface

Pin	Name	Comment
1	V+	3.3V
2	DGND	Ground
3	SCK	SPI: Clock
4	SDO	SPI: Data Out
5	SDI	SPI: Data In
6	SS	SPI: Slave Select

Table 4-28: J24 -PROM-PROG Config Prom SPI program interface

4.2 List of Oscillators, Switches and LED's

Name	Function	Description
X1	OSC_MAIN	Oscillator for main ASIC clock, SMD type, 3.3V, 50MHz
X2	OSC_USER	Alternative User oscillator for main ASIC clock, DIL8 socket, 3.3V
X3	OSC_PCI	Oscillator for PCI interfaces, 3.3V, 33.3MHz
X4	OSC_USB	Oscillator for USB interfaces, 3.3V, 19.2MHz
Y1	XTAL_RTC	32.768kHz crystal for I2C Real Time Clock

Table 4-29: List and definition of Oscillators

Name	Function	Description
D1	POWER (3.3V)	Power indicator
D2	ERRORN	Leon processor in 'ERROR' mode
D3-D10	GPIO[27..34]	LED indicators for GPIO[27..34]
D11	DSUACT	LED indicator for DSU Active
D12	USB_FAULT1	Current Overload Fault on USB-Host 1
D13	USB_FAULT0	Current Overload Fault on USB-Host 2
D11	PROM_BUSY	Prom Write/Erase in Progress
D4	WDOG	Watchdog indicator

Table 4-30: List and definition of PCB mounted LED's

Name	Function	Description
S1	GPIO24	Push button switch connected to GPIO24 (Default logic '0')
S2	GPIO25	Push button switch connected to GPIO25 (Default logic '0')
S3	GPIO26	Push button switch connected to GPIO26 (Default logic '0')
S4	GPIO[23..16]	8 pole DIP switch connected to GPIO[23..16] (Logic '1' when 'open')
S5	DSU_BREAK	Push button DSU_BREAK switch
S6	RESET	Push button RESET switch
S7	ETH_EDCL_ADDR	4 pole DIP switch to configure ETH EDCL address

Table 4-31: List and definition of Switches

4.3 List of Jumpers

Name	Function	Type	Description
JP1	CLOCK_CFG	1X3 0.1"Header	Connects either X1 to X2 oscillator to Main oscillator i/p
JP2	WDOG_EN	1X2 0.1"Header	Install to allow Watchdog signal to reset board
JP3	RESET	1X2 0.1"Header	Pins for external RESET switch
JP4	DSU-BREAK	1X2 0.1"Header	Pins for external DSU BREAK switch
JP5	+3.3V	1X2 0.1"Header	Test/Power header (Pin 1 = DGND, Pin2 = +3.3V)
JP6	+5V	1X2 0.1"Header	Test/Power header (Pin 1 = DGND, Pin2 = +5V)
JP7	CAN1-Term	2X2 0.1"Header	Configure End Node Termination for CAN-1 I/F
JP8	CAN0-Term	2X2 0.1"Header	Configure End Node Termination for CAN-0 I/F
JP9	I2CS-Pullup	2X2 0.1"Header	Install 1-2 and 3-4 to provide 10k pull-ups on SCL/SDA
JP10	I2CM1-Pullup	2X2 0.1"Header	Install 1-2 and 3-4 to provide 10k pull-ups on SCL/SDA
JP11	ASIC-SPI	2X4 0.1"Header	Install 1-2, 3-4, 5-6, 7-8 except if U2 Prom is being programmed, when all are removed

Table 4-32: List and definition of PCB Jumpers
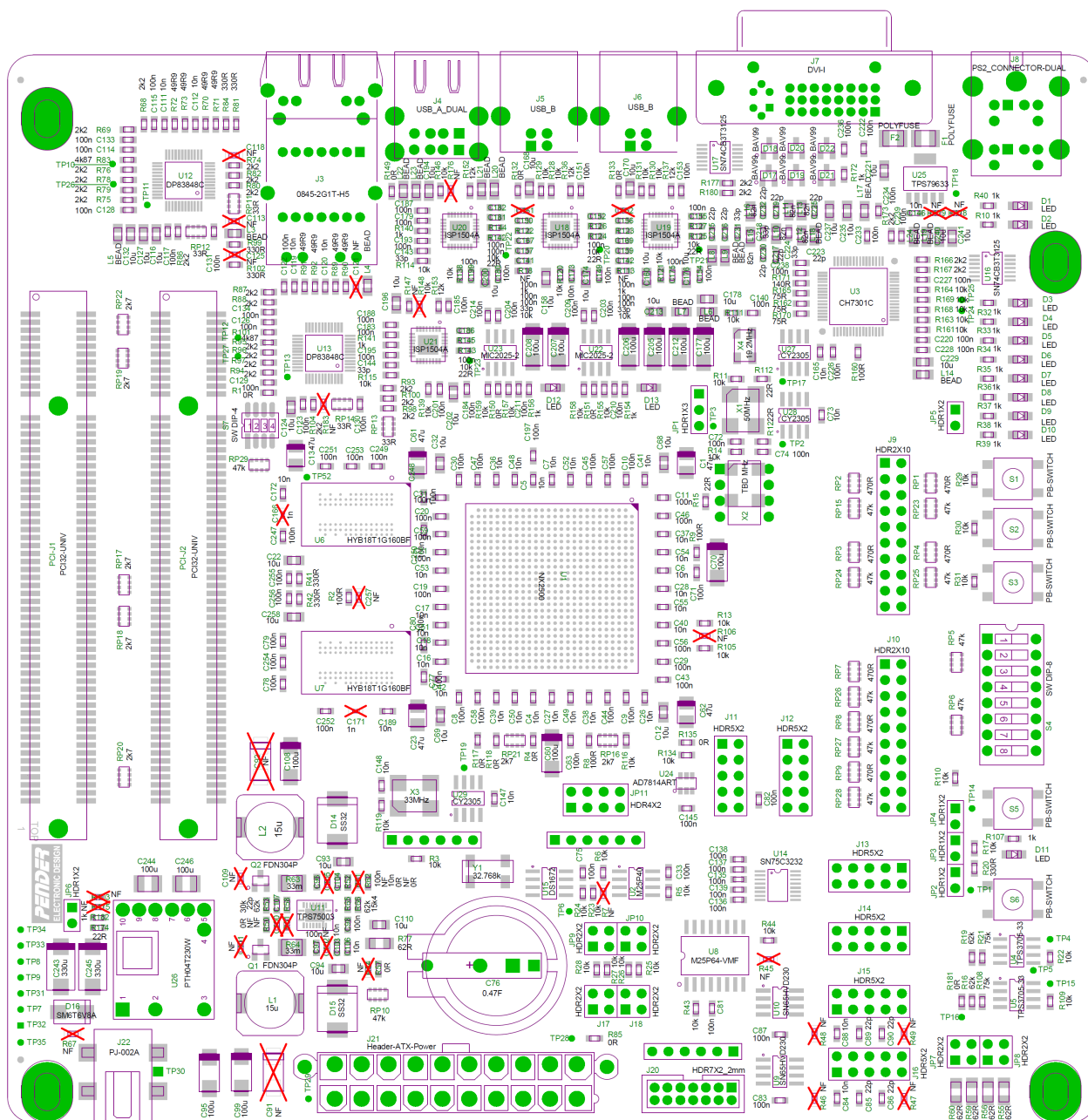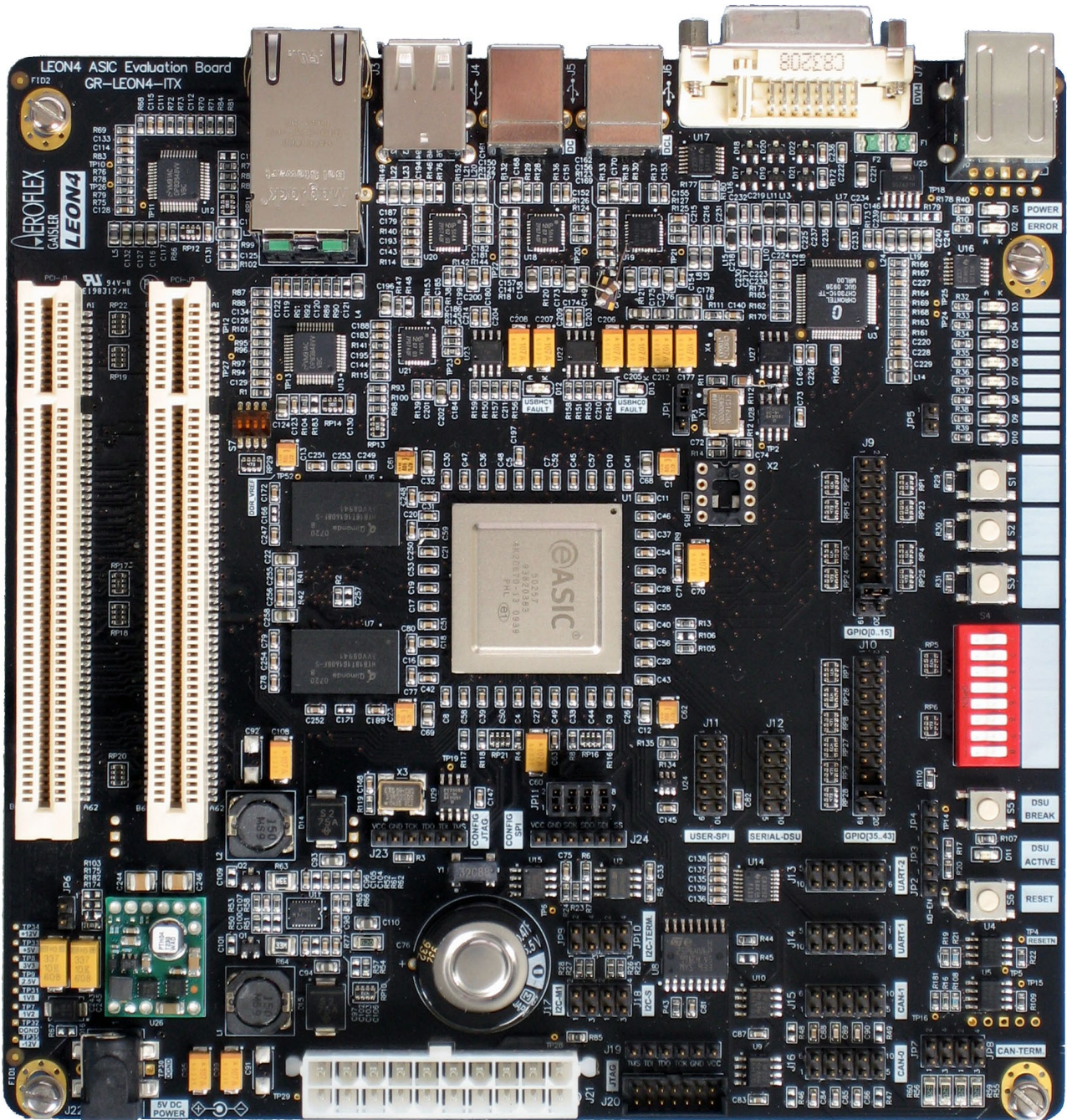
(for details refer to schematic, RD 1)

Figure 4-3: PCB Top View

Figure 4-4: GR-LEON4-ITX Assembly Photo (Top View)